

ASX RELEASE

15 January 2025

4DS SUCCESSFULLY COMPLETES FIFTH PLATFORM LOT

Key Highlights:

- **4DS successfully completes testing and characterization of the Fifth Platform Lot**
- **Characterization of the Fifth Platform Lot de-risks the manufacture of the 20nm memory cell array incorporated in the Sixth Platform Lot**
- **The Sixth Platform Lot will scale the 4DS memory cell array from 60nm cells to 20nm cells (9x smaller) and position the 4DS ReRAM technology as a potential generational memory**

Further to the announcement on 17 December 2024, 4DS Memory Limited has now successfully completed characterization and testing of the Fifth Platform Lot. The Company and the imec engineering team will now focus on the manufacture of the Sixth Platform Lot 20nm memory cell array.

The purpose of the Fifth Platform Lot was to optimize the construction process of memory cell arrays to de-risk the manufacturing of the first 4DS 20nm memory cell array incorporated in the Sixth Platform Lot.

Using the proven cell size of 60nm array (demonstrated in the Fourth Platform Lot), the Fifth Platform Lot sought to uncover any processing issues that could arise when adjusting the memory cell stack necessary for successful construction of the 20nm memory cell array in the Sixth Platform Lot.

After extensive electrical testing including chemical and physical cross-sectional analysis, key areas of optimisation were identified and shared with the imec engineering team working on the Sixth Platform Lot.

The key process learnings from the Fifth Platform Lot that are necessary for scaling of the memory cell array from 60nm cells to 20nm cells (9 times smaller in area) and that are now in the process of being implemented to the Sixth Platform Lot are:

- Memory cell array patterning and etching: new process tuning modifications for the construction of 20nm cells.
- Memory stack adjustment: the advanced memory stacks which are necessary for the construction of 20nm cells have shown functionality and which de-risks the Sixth Platform Lot with similar memory cell stack constructions.
- Memory array process integration: the best options of the post-patterning backend processes of the advanced memory cells were selected and implemented to the Sixth Platform Lot.

These new learnings and optimizations from the Fifth Platform Lot are critically important for the successful processing of 4DS's first 20nm memory cell array in the Sixth Platform Lot, expected to be manufactured and analysed in 1H 2025. If the Company is successful in scaling from a 60nm memory cell to 20nm memory cell array, then the Sixth Platform Lot will position 4DS' area-based Interface Switching ReRAM technology as a potential generational memory.

4DS Interactive Investor Hub

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Authorised for release by the Board.

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About 4DS

4DS Memory Limited (ASX: 4DS), with facilities located in Silicon Valley, is a semiconductor technology company bringing high bandwidth, high endurance, persistent non-volatile memory to advanced CMOS process nodes. Its technology, known as Interface Switching ReRAM, features tunable persistence and low energy per bit for today's most challenging compute intensive and AI processor applications. Established in 2007, 4DS owns a patented IP portfolio, comprising 34 USA patents, and is the first company to develop PCMO ReRAM, on an advanced CMOS processing node. 4DS has three important industry relationships; a development agreement with Belgium based imec, a world leading research and innovation hub in nano electronics and digital technologies; a design agreement with Infineon Technologies AG, Germany's largest semiconductor manufacturer and one of the ten largest semiconductor manufacturers worldwide; and a joint development agreement with Western Digital subsidiary HGST, a global leader in storage solutions.

For more information, please visit www.4dsmemory.com.

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